Patent claims

1. A semiconductor device with a plastic package molding compound (2), a semiconductor chip (3) and a leadframe (4), the semiconductor chip (3) being embedded with one of its two upper sides (7, 8) and its peripheral sides (5, 6) in the plastic package molding compound (2), and the other of its two upper sides (7, 8) being surface-mounted on an upper side (9) of the leadframe (4), and the region of the upper side (9) of the leadframe (4) that is not covered by the semiconductor chip (3) being covered by the plastic package molding compound (2), and a continuous elastic adhesive layer (11) being arranged between the plastic package molding compound (2) and the leadframe (4), and between the semiconductor chip (3) and the leadframe (4), on the upper side (9) of the leadframe (4).

2. The semiconductor device as claimed in claim 1, characterized in that peripheral regions (12) of the semiconductor device (1) are free of the elastic adhesive layer (11).

3. The semiconductor device as claimed in claim 2, characterized in that the peripheral regions (12) of the semiconductor device (1) that are kept free of the adhesive layer (11) comprise elastic metal layers (13).

4. The semiconductor device as claimed in claim 3, characterized in that the metal layers (13) comprise a copper layer (14) of a copper alloy arranged on the leadframe (4) and a gold layer (15) of a gold alloy applied on top of it.

5. The semiconductor device as claimed in claim 3, characterized in that the metal layers (13)

comprise a copper layer (14) of a copper alloy arranged on the leadframe (4) and a silver layer of a silver alloy applied on top of it.

6. The semiconductor device as claimed in claim 3, characterized in that the metal layers (13) comprise a copper layer (14) of a copper alloy arranged on the leadframe (4) and an aluminum layer of an aluminum alloy applied on top of it.

7. The semiconductor device as claimed in one of claims 3 to 6, characterized in that the width (b) of the metal layers (13) in the peripheral regions (12) of the semiconductor device (1) are adapted to the width of sawing tracks in such a way that the elastic adhesive layer (11) is not exposed to the sawing process in the production of peripheral sides of the semiconductor device (1).

8. A panel, which has device positions with semiconductor devices (1, 10) arranged in rows and columns, as claimed in one of claims 1 to 7.

9. A method for producing a panel with a plastic package molding compound (2), semiconductor chips (3) and a leadframe (4) in a number of semiconductor device positions, the method having the following method steps:

- production of a leadframe (4) with device positions arranged in rows and/or columns;
- application of an elastic adhesive layer (11), covering both the region of the intended semiconductor chip (3) and the region of the intended plastic package molding compound (2) on an upper side (9) of the leadframe (4) in the device positions;

- adhesive attachment of semiconductor chips (3) onto the adhesive layer (11) in the device positions,
- establishment of electrical connections (16) between contact areas (20, 21) of the semiconductor chip (3) and the leadframe (4) in the device positions;
- application of a plastic package molding compound (2) to the adhesive layer (11) while embedding the semiconductor chips (3) and while forming a panel with a number of semiconductor device positions.

10. The method as claimed in claim 9, characterized in that a pattern of metal layers (13), which covers more than the width of the sawing tracks with the metal layers (13), and preferably has a width in the range of 1.2 times to 3 times the width of the sawing tracks, is applied to the leadframe (4) before the application of the adhesive layer (11).

11. The method as claimed in claim 9 or claim 10, characterized in that a central opening (18) for a bonding channel (19) is introduced in the device positions of the leadframe (4) when the leadframe (4) is produced.

12. The method as claimed in claim 9 or claim 11, characterized in that the semiconductor chip (3) is applied with its active upper side (7) to the adhesive layer (11) of the leadframe (4) while aligning contact areas (20, 21) of the semiconductor chip (3) arranged in two rows over the central opening (18) of the leadframe (4), and bonding wires (22) for connecting the contact areas (20, 21) of the semiconductor chip (3) to bonding fingers (23) of a wiring structure (24) are

attached on the rear side (25) of the leadframe (4) in the device positions.

13. The method as claimed in claim 9 or claim 12, characterized in that the bonding wires (22) in the central opening (18) are embedded in plastic package molding compound (2).

14. A method for producing a semiconductor device (1, 10), the method having the following further method steps:
- production of a panel as claimed in one of claims 10 to 13;
- application of external contacts (26) to the panel;
- dividing up of the panel into individual semiconductor devices (1) along sawing tracks.

15. A method for producing semiconductor devices (1, 10), the method having the following further method steps:
- production of a panel as claimed in one of claims 10 to 13;
- dividing up of the panel into individual semiconductor devices (1) along sawing tracks;
- application of external contacts (26) to the individual semiconductor device (1).